WHAT IS CLAIMED IS:

1. An ion sensitive field effect transistor (ISFET) comprising:

a non-single-crystal-silicon-base substrate;

a polysilicon layer formed above the non-single-crystal silicon-base substrate;

a source and a drain formed in the polysilicon layer, with a predetermined channel region formed between the source and the drain in the polysilicon layer;

an insulating layer with a first contact hole and a second contact hole, formed above the polysilicon layer;

a first electrode and a second electrode electrically couple to the source and the drain by the first contact hole and the second contact hole, respectively;

a passivation layer formed above the insulating layer covering the first electrode and the second electrode, wherein the passivation layer comprise an opening partially exposing a surface of the insulating layer

above the predetermined channel region; and

an ion sensitive gate formed in the opening above the insulating layer.

2. The ISFET according to claim 1, wherein the passivation layer is epoxy resin.

3. The ISFET according to claim 1, wherein the non-single-crystal silicon-base substrate is a glass substrate.

4. The ISFET according to claim 1, wherein the non-single-crystal silicon-base substrate is a plastic substrate.

5. The ISFET according to claim 1, wherein the non-single-crystal silicon-base substrate is an insulation substrate.

6. The ISFET according to claim 1, wherein the insulating layer is a silicon oxide layer.

7. The ISFET according to claim 1, wherein the first electrode and the second electrode are metal electrodes.

8. A fabrication method of an ion sensitive field effect transistor (ISFET) comprising:

providing a non-single-crystal silicon-base substrate;

forming a polysilicon layer above the non-single-crystal silicon-base substrate;

forming a source and a drain in the polysilicon layer, with a predetermined channel region formed between the source and the drain in the polysilicon layer;

forming an insulating layer with a first contact hole and a second contact hole above the polysilicon layer, wherein the first contact hole and the second contact hole partially expose the source and the drain exposed, respectively;

forming a first electrode and a second electrode, wherein the first electrode and the second electrode are electrically coupled with the source and the drain by the first contact hole and the second contact hole, respectively;

forming a passivation layer with an opening above the insulating layer, wherein the passivation layer covers the first electrode and the second electrode, and the opening partially exposes the insulating layer above

the predetermined channel region; and

forming an ion sensitive gate in the opening above the insulating layer.

9. The method according to claim 8, wherein the step of forming a source and a drain in the polysilicon layer further comprises:

defining a front side of the polysilicon layer so as to form two predetermined doped-regions;

doping the two predetermined doped-regions so as to form the source and the drain correspondingly.

10. The method according to claim 8, wherein the non-single-crystal silicon-base substrate is a glass substrate.

11. The method according to claim 8, wherein the non-single-crystal silicon-base substrate is a plastic substrate.

12. The method according to claim 8, wherein the non-single-crystal silicon-base substrate is an insulation substrate.

13. The method according to claim 8, wherein the insulating layer is a silicon oxide layer.

14. The method according to claim 8, wherein the first electrode and the second electrode are two metal electrodes.

15. The method according to claim 8, wherein the passivation layer is epoxy resin.

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